**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended) An electronic circuit arrangement comprising:

a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal; and

an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, wherein the asynchronous processor remains dormant in the absence of a clock failure event, wherein the asynchronous processor does not receive and is not dependent on any clock signal.

2. (original) An electronic circuit arrangement as claimed in claim 1, characterized in that the asynchronous processor comprises an interrupt input for receiving the error signal and is further arranged to execute software instructions upon reception of the error signal.

3. (original) An integrated circuit comprising an electronic circuit arrangement as claimed in claim 1.

4. (original) A bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1.

5. (previously presented) A bus station as claimed in claim 4, characterized in that the bus station is a bus station for use in a LIN bus system.

6. (currently amended) A method for bringing an electronic circuit arrangement into a predetermined state, the method comprising:

detecting an absence of a clock signal using a clock fail circuit;

generating an error signal in response to the absence of the clock signal; and

bringing the electronic circuit arrangement into the predetermined state using an asynchronous processor within the electronic circuit arrangement, wherein the asynchronous processor remains dormant in the absence of a clock failure event, wherein the asynchronous processor does not receive and is not dependent on any clock signal.

7. (canceled)

8. (previously presented) An electronic circuit arrangement as claimed in claim 1, wherein the asynchronous processor does not consume power in the absence of receiving the error signal.

9. (previously presented) A method as claimed in claim 6, further comprising the asynchronous processor executing software instructions upon reception of the error signal.

10. (canceled)

11. (previously presented) A method as claimed in claim 6, wherein the asynchronous processor does not consume power in the absence of receiving the error signal.

12. (new) An electronic circuit arrangement comprising:

a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal; and

an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, wherein the asynchronous processor remains dormant in the absence of a clock failure

event, wherein the asynchronous processor does not consume power in the absence of receiving the error signal.

13. (new) An electronic circuit arrangement as claimed in claim 1, characterized in that the asynchronous processor comprises an interrupt input for receiving the error signal and is further arranged to execute software instructions upon reception of the error signal.

14. (new) An integrated circuit comprising an electronic circuit arrangement as claimed in claim 1.

15. (new) A bus station for use in a bus system comprising an electronic circuit arrangement as claimed in claim 1.

16. (new) A bus station as claimed in claim 4, characterized in that the bus station is a bus station for use in a LIN bus system.